

1 We claim:

2

3 1) A process for transmitting a packet having a header  
4 and variable length payload on a communications interface  
5 comprising the steps:

6 a first step of sending IDLE symbols until a  
7 synchronization time has passed;

8 a second step of sending said packet including a START  
9 symbol and TYPE field identifying the format of said payload  
10 including an FCS sequence;

11 a third step of sending said variable length payload;

12 a fourth step of sending a terminator including an END  
13 symbol indicating end of transmission of said packet;

14 a fifth step of sending IDLE symbols if next said  
15 packet is not ready to transmit, or returning to said second  
16 step if said next packet is ready to transmit.

17

18 2) The process of claim 1 wherein said TYPE field  
19 uniquely identifies said payload format, said format  
20 including Ethernet packets, native IP packets, ATM cells,  
21 and control packets.

22

23 3) the process of claim 2 wherein said header further  
24 includes declaration fields for at least one of BPDU,  
25 PRIORITY, VLAN\_ID, and an application specific field.

1

2           4) The process of claim 3 wherein said BPDU field is 1  
3 bit in size.

4

5           5) The process of claim 3 wherein said PRIORITY field  
6 is 3 bits in size.

7

8           6) The process of claim 3 wherein said VLAN\_ID field is  
9 12 bits in size.

10

11           7) The process of claim 3 wherein said application  
12 specific field is 32 bits in size.

13

14           8) The process of claim 3 wherein said header  
15 comprises, in sequence, said START symbol, said BPDU field,  
16 said TYPE field, said PRIORITY field, said VLAN\_ID field,  
17 and said application-specific field.

18

19           9) The process of claim 1 wherein a plurality n of data  
20 lanes carry said header, said payload, and said END symbol.

21

22           10) the process of claim 9 wherein

1       said second step comprises transmitting said header  
2 across said n data lanes until all said header information  
3 has been sent;

4       said third step comprises transmitting said variable  
5 length payload, wherein during a final payload cycle, said  
6 payload ends on said data lane m;

7       for the case where  $m < n$ , said fourth step includes  
8 sending on said final payload cycle said END symbol on lane  
9 m+1, and said IDLE symbol on any available data lanes m=n+2  
10 through n;

11       for the case where  $m = n$ , said fourth step comprises  
12 sending said END symbol on said data lane 0, and said IDLE  
13 symbol on said data lane 1 through said data lane n.

14

15       11) The process of claim 10 where  $n = 8$ .

16

17       12) The process of claim 10 where  $n = 4$ .

18

19       13) The process of claim 10 where  $n = 2$ .

20

21       14) the process of claim 9 where  $n = 1$ , and

1       said second step comprises transmitting said header on  
2       said data lane until all said header information has been  
3       sent;

4       said third step comprises transmitting said variable  
5       length payload on said data lane,

6       said fourth step comprises sending said END symbol on  
7       said data lane.

8

9       15) The process of claim 10 wherein at least one said  
10      data lane comprises a serial electrical link.

11

12      16) The process of claim 10 wherein at least one said  
13      data lane comprises a parallel electrical link.

14

15      17) The process of claim 10 wherein at least one said  
16      data lane comprises one or more serial or parallel optical  
17      links.

18

19      18) The process of claim 10 wherein said first step  
20      comprises the transmission of said IDLE symbols on all said  
21      n data lanes.

22

1        19) The process of claim 18 wherein said IDLE symbols  
2 are transmitted across all said n data lanes when there is  
3 no said packet data available to transmit.

4

5        20) The process of claim 19 wherein successive data  
6 lane cycles toggle successively between the states odd and  
7 even.

8

9        21) The process of claim 20 wherein said IDLE symbols  
10 transmitted comprise IDLE\_ODD symbols during said odd state,  
11 and IDLE\_EVEN symbols during said even state.

12

13        22) A communication interface comprising n data lanes,  
14 said interface sequentially transmitting a header  
15 distributed across a plurality of said data lanes, a  
16 variable amount of payload data distributed across a  
17 plurality of said n data lanes.

18

19        23) The communication interface of claim 22 wherein  
20 said transmission of said header includes transmitting a  
21 START symbol on first said data lane, and the transmission  
22 of said payload data is followed by an END symbol on at  
23 least one said data lane.

24

1        24) The communication interface of claim 23 wherein  
2        said transmission of said payload data includes transmitting  
3        data across said n data lanes up to data lane m, where  $m \leq$   
4        n.

5

6        25) The communication interface of claim 24 wherein if  
7        said  $m < n$ , said END symbol is transmitted on data lane  $m+1$ ,  
8        and if said  $m=n$ , said END symbol is transmitted on data lane  
9        0.

10

11       26) The communication interface of claim 25 wherein  
12       each said data lane is identified by the alternating states  
13       of odd and even cycles.

14

15       27) The communication interface of claim 26 wherein  
16       said IDLE symbol is IDLE\_EVEN during said even cycle and  
17       IDLE\_ODD during said odd cycle.

18

19       28) The communication interface of claim 27 wherein all  
20       said data lane 0 through data lane n transmit IDLE\_EVEN  
21       during said even cycles, and IDLE\_ODD during said odd  
22       cycles.

23

1        29) The communication interface of claim 28 where  
2    IDLE\_EVEN or IDLE\_ODD are transmitted after said END symbol  
3    at least once during every interval  $t_{elasticity}$ .

4  
5        30) The communication interface of claim 29 where  
6     $t_{elasticity} = T_{transmit} * clk\_offset$ ,  
7        where  
8         $T_{transmit}$  = time since last IDLE transmittal  
9         $clk\_offset = (maximum\ Transmit\ clock\ rate - minimum$   
10     $receive\ clock\ rate)/(minimum\ receive\ clock\ rate)$ .

11  
12        31) A transmit processor comprising:  
13        a busy input;  
14        a transmit buffer/controller accepting packet data  
15    comprising a header and a payload as input, arranging said  
16    packet data into a plurality n of data lanes, and delivering  
17    to each said data lane unencoded transmit data and a control  
18    signal, whereby when said control signal is asserted, said  
19    unencoded transmit data includes at least one of the values  
20    START, END, IDLE, IDLE\_BUSY and when said control signal is  
21    not asserted, said transmit data includes said packet data;  
22        a plurality n of transmit encoders, each having an  
23    input and an output, each of said transmit encoder inputs  
24    uniquely coupled to one of said transmit buffer/controller  
25    data lanes, said transmit encoder input comprising said

1 unencoded transmit data and said control signal, said  
2 transmit encoder output producing a unique encoded output  
3 value for each said unencoded transmit data value when said  
4 control signal is not asserted, and producing a unique  
5 encoded output values for each unencoded transmit data  
6 START, END, IDLE, and IDLE\_BUSY when said control signal is  
7 asserted;

8 a plurality n of transmit serializers, each having an  
9 input uniquely coupled to one of said transmit encoder  
10 outputs, said transmit serializers outputting a single  
11 serial stream of data from said transmit serializer input;

12 wherein said transmit buffer/controller sends said  
13 header by outputting on said first data lane the asserted  
14 said control and said unencoded transmit data START, and  
15 simultaneously outputs the remainder of said header on said  
16 remaining data lanes accompanied by said unasserted control  
17 signal for each said data lane,

18 thereafter and on each successive cycle said transmit  
19 buffer/controller distributes said payload data on all said  
20 data lanes and sends it to said transmit encoder with said  
21 unasserted control signal accompanied by said payload data,  
22 until unsent said payload data can not fully span said n  
23 data lanes,

24 thereafter said transmit buffer/controller sends the  
25 last said payload data on each said data lane with



1 associated said control signal unasserted, with following  
2 said data lane having said control signal asserted  
3 accompanied by said unencoded data END, and the remaining  
4 said data lanes having said control signal asserted  
5 accompanied by said unencoded data IDLE.

6

7 32) The transmit processor of claim 31 wherein each  
8 said transmit cycle has the state odd or even, and said IDLE  
9 comprises an IDLE\_EVEN sent on said even cycles or an  
10 IDLE\_ODD sent on said odd cycle.

11

12 33) The transmit processor of claim 32 wherein each  
13 successive transmit cycle alternates between odd or even,  
14 said IDLE\_EVEN is sent during even cycles, and IDLE\_ODD is  
15 sent during odd cycles.

16

17 34) The transmit processor of claim 32 wherein said  
18 IDLE comprises an IDLE when said busy input is not asserted,  
19 or a IDLE\_BUSY when said busy input is asserted.

20

21 35) The transmit processor of claim 34 wherein said  
22 IDLE comprises an IDLE\_EVEN\_BUSY during said even cycle when  
23 said busy input is asserted, an IDLE\_EVEN during said even  
24 cycle when said busy input is not asserted, an IDLE\_ODD\_BUSY  
25 during said odd cycle when said busy input is asserted, and

1 an IDLE\_ODD during said odd cycle when said busy is not  
2 asserted.

3

4 36) The transmit processor of claim 35 wherein said  
5 transmit encoder comprises an 8B/10B encoder.

6

7 37) The transmit processor of claim 36 wherein the  
8 number of said data lanes  $n = 8$ .

9

10 38) The transmit processor of claim 36 wherein the  
11 number of said data lanes  $n = 4$ .

12

13 39) The transmit processor of claim 36 wherein the  
14 number of said data lanes  $n = 2$ .

15

16 40) The transmit processor of claim 36 wherein the  
17 number of said data lanes  $n = 1$ .

18

19 41) The transmit processor of claim 36 wherein the 10B  
20 coding value for symbol START is K27.7.

21

22 42) The transmit processor of claim 36 wherein the 10B  
23 coding value for symbol END is K29.7.

24

1       43) The transmit processor of claim 36 wherein the 10B  
2 coding value for symbol IDLE\_EVEN is K28.5.

3

4       44) The transmit processor of claim 36 wherein the 10B  
5 coding value for symbol IDLE\_ODD is K23.7.

6

7       45) The transmit processor of claim 36 wherein the 10B  
8 coding value for symbol IDLE\_EVEN\_BUSY is K28.1.

9

10       46) The transmit processor of claim 36 wherein the 10B  
11 coding value for symbol IDLE\_ODD\_BUSY is K28.0.

12

13       47) The transmit processor of claim 36 wherein the 10B  
14 coding values for the symbols START, END, IDLE\_EVEN,  
15 IDLE\_EVEN\_BUSY, IDLE\_ODD, and IDLE\_ODD\_BUSY have unique  
16 values when compared to any coded 10B data value.

17

18       48) The transmit processor of claim 47 wherein the 10B  
19 coding values for the symbols START, END, IDLE\_EVEN,  
20 IDLE\_EVEN\_BUSY, IDLE\_ODD, and IDLE\_ODD\_BUSY are separated by  
21 hamming distance 2.

22

23       49) A receive processor comprising:

1       a plurality n of receive deserializers each accepting  
2   as input a serial stream of encoded data and outputting  
3   deserialized encoded data;  
4       a plurality n of receive decoders each uniquely coupled  
5   to and accepting as input said deserialized encoded data and  
6   providing as output decoded data and decoded control  
7   signals, said decoded data including at least on of the  
8   values START, END, and IDLE when said control signal is  
9   asserted;  
10      a receive buffer/controller for the formation of data  
11   packets, said buffer/controller having a plurality n of  
12   inputs, each uniquely coupled to said decoded data and said  
13   decoded control, said buffer/controller having a busy output  
14   and a data output, said receive buffer/controller awaiting  
15   START on said first lane with associated control signal  
16   asserted, and storing a header on the remaining said data  
17   lanes when said START is received, and transferring to said  
18   data output all subsequent data while said control signal is  
19   unasserted for all said data lanes, and upon receipt of said  
20   END accompanied by the assertion of said associated control  
21   signal on any data lane, transferring said decoded data to  
22   said data output all said received data up to but not  
23   including said data lane having said control signal END.  
24

1           50) The receive processor of claim 49 wherein said IDLE  
2 comprises the symbols IDLE\_EVEN, IDLE\_ODD, IDLE\_EVEN\_BUSY,  
3 and IDLE\_EVEN\_ODD.

4

5           51) The receive processor of claim 50 including a busy  
6 signal wherein the reception of IDLE\_EVEN\_BUSY or  
7 IDLE\_ODD\_BUSY causes said receive processor to assert said  
8 busy output.

9

10          52) The receive processor of claim 49 wherein said  
11 receive decoder uses a 10B/8B decoding method for converting  
12 said encoded data into said decoded data.

13

14          53) The receive processor of claim 52 wherein each  
15 receive deserializer achieves synchronization using the  
16 symbols IDLE\_EVEN and IDLE\_ODD.

17

18          54) the receive processor of claim 52 wherein the 10B  
19 coding value for symbol START is K27.7.

20

21          55) The receive processor of claim 52 wherein the 10B  
22 coding value for symbol END is K29.7.

23

24          56) The receive processor of claim 52 wherein the 10B  
25 coding value for symbol IDLE\_EVEN is K28.5.

1

2       57) The receive processor of claim 52 wherein the 10B  
3 coding value for symbol IDLE\_ODD is K23.7.

4

5       58) The receive processor of claim 52 wherein the 10B  
6 coding value for symbol IDLE\_EVEN\_BUSY is K28.1.

7

8       59) The receive processor of claim 52 wherein the 10B  
9 coding value for symbol IDLE\_ODD\_BUSY is K28.0.

10

11

12       60) The receive processor of claim 52 wherein the 10B  
13 encoded values for the symbols START, END, IDLE\_EVEN and  
14 IDLE\_ODD have unique values when compared to any other  
15 encoded 10B data value.

16

17       61) The receive processor of claim 60 wherein the 10B  
18 coding values for the symbols START, END, IDLE\_EVEN, and  
19 IDLE\_ODD are separated by hamming distance 2.

20

21       62) The receive processor of claim 49 wherein the  
22 number of data lanes  $n = 8$ .

23

24       63) The receive processor of claim 49 wherein the  
25 number of data lanes  $n = 4$ .

1  
2       64) The receive processor of claim 49 wherein the  
3 number of data lanes  $n = 2$ .

4  
5       65) The receive processor of claim 49 wherein the number of  
6 data lanes  $n = 1$ .

7  
8       66) A communications interface for sending or receiving  
9 a packet, said packet comprising, in sequence, a header,  
10 variable length payload, and a terminator;

11       said header including a START symbol and a TYPE field  
12 identifying the format of said payload;

13       said terminator including an END symbol;

14       wherein said START symbol is transmitted first,  
15 followed by the remainder of said header, followed by said  
16 variable length packet data, followed by said terminator.

17  
18       67) The interface of claim 66 wherein said TYPE field  
19 uniquely identifies said payload format, said format  
20 including Ethernet packets, ATM cells, and control packets.

21  
22       68) the interface of claim 67 wherein said header  
23 further includes declaration fields for at least one of  
24 BPDU, PRIORITY, VLAN\_ID, and an application specific field.

